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FIG. 1

$$m = a \times b \times c$$

$$S1 : Dy_d, Dy_{dc+d}, \dots, Dy_{(a-1)bc+d}$$

$$S2 : Dy_{b+d}, Dy_{bc+b+d}, \dots, Dy_{(a-1)bc+b+d}$$

$$\vdots$$

$$S_{c-1} : Dy_{(c-2)b+d}, Dy_{(c-2)b+bc+d}, \dots, Dy_{(c-2)b+(a-1)bc+d}$$

$$S_c : Dy_{(c-1)b+d}, Dy_{(c-1)b+bc+d}, \dots, Dy_{(c-1)b+(a-1)bc+d}$$

(d IS A NATURAL NUMBER OF 1~b)

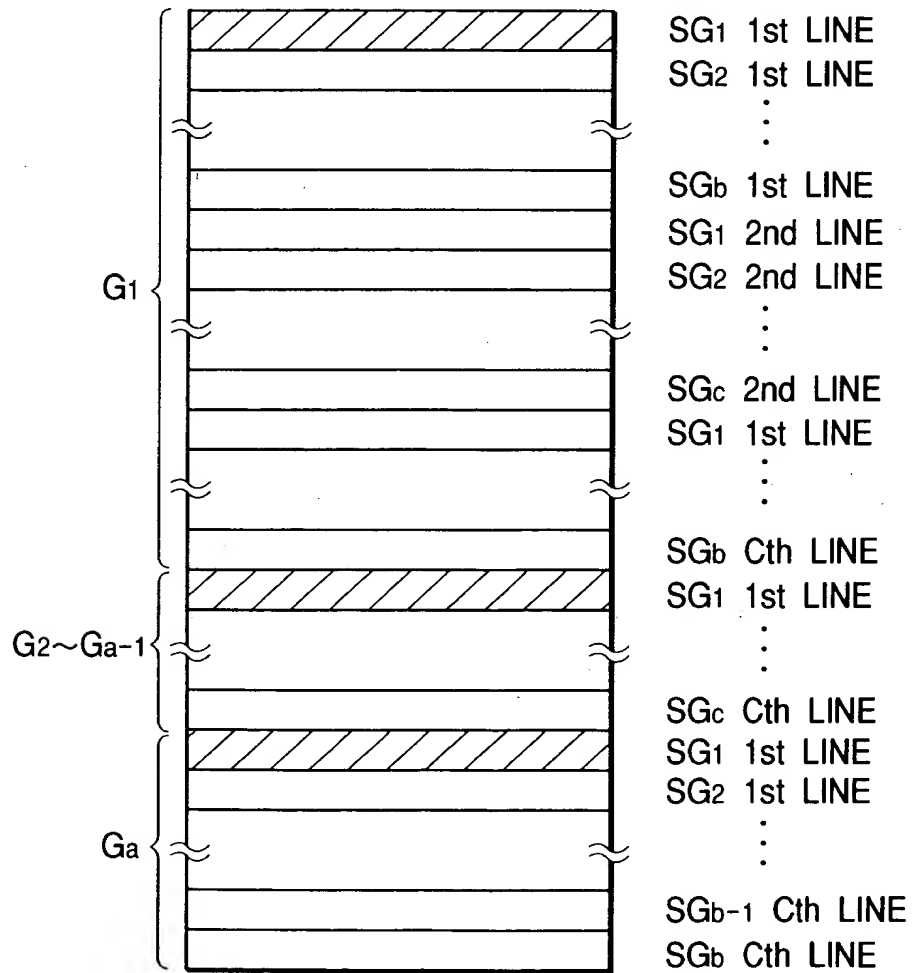


FIG. 2A

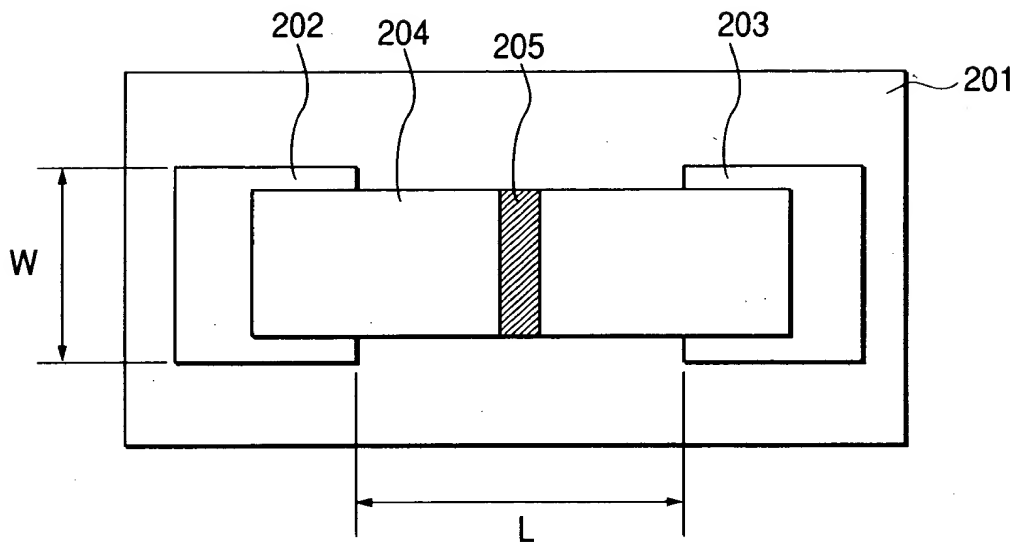


FIG. 2B

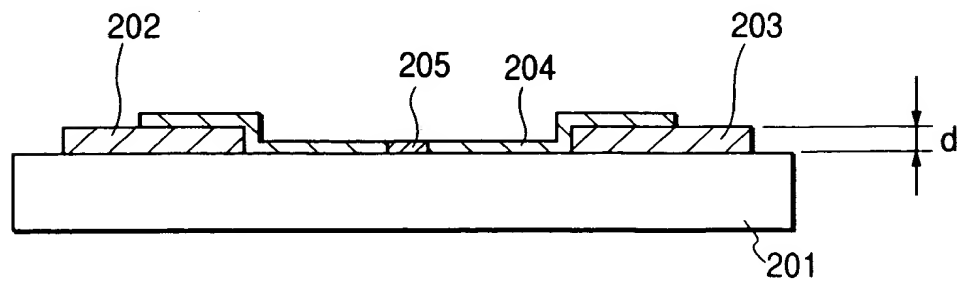


FIG. 3A

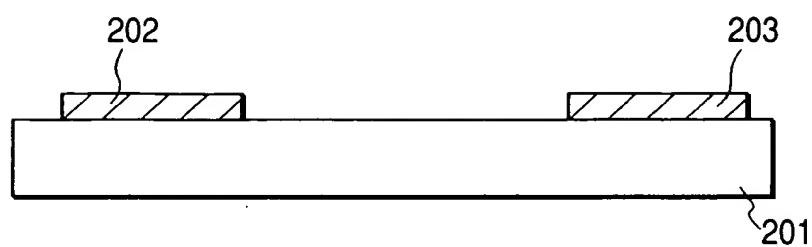


FIG. 3B

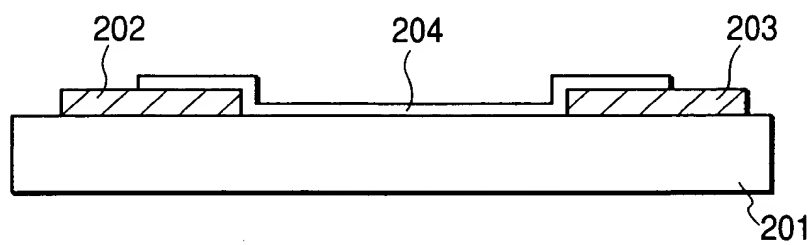


FIG. 3C

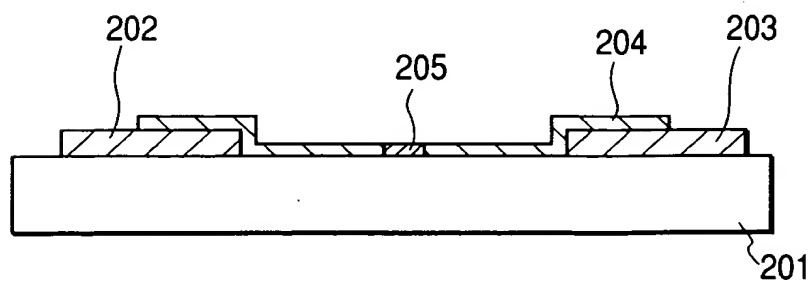


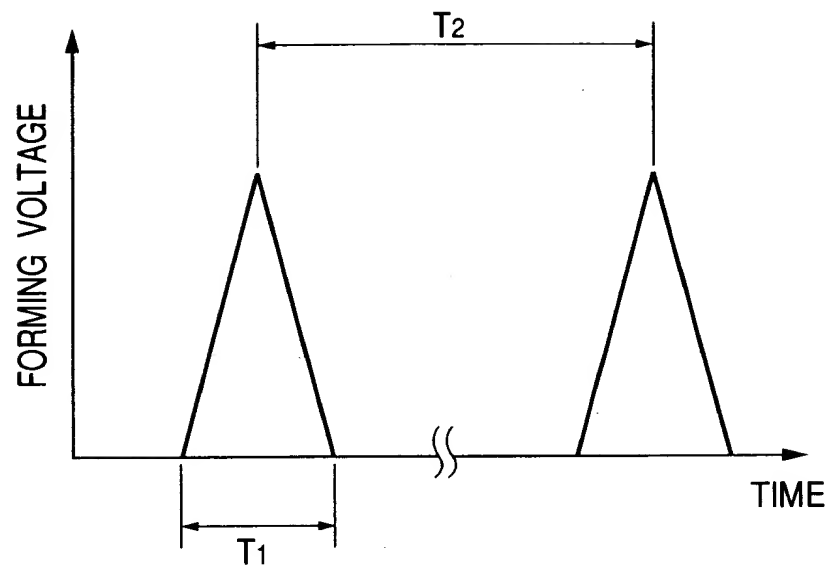
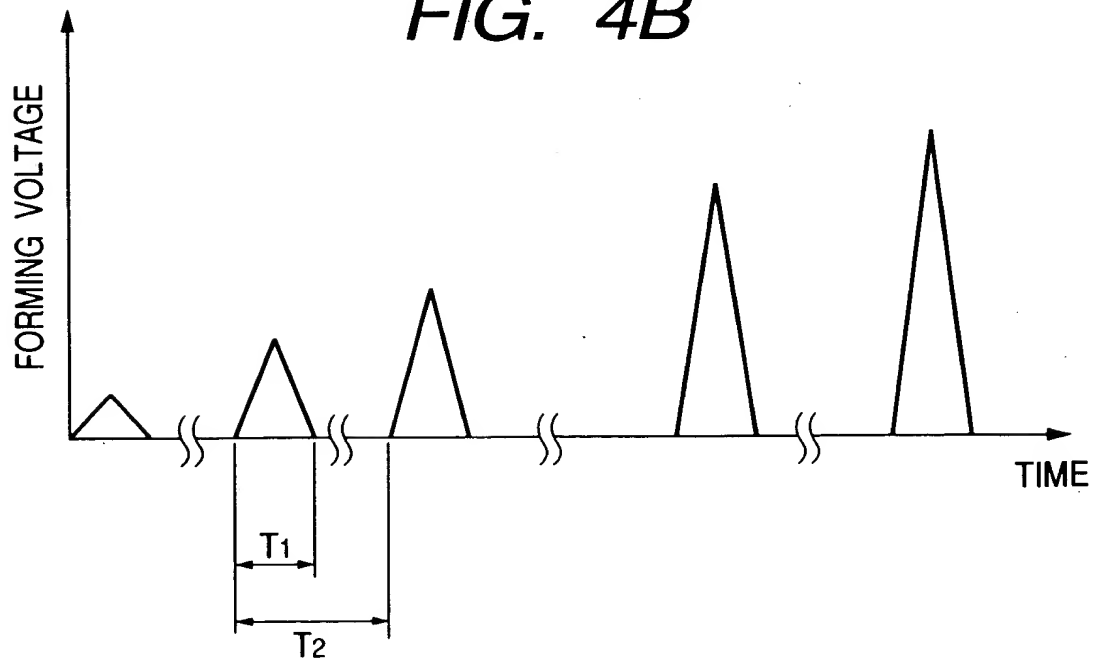
FIG. 4A**FIG. 4B**

FIG. 5

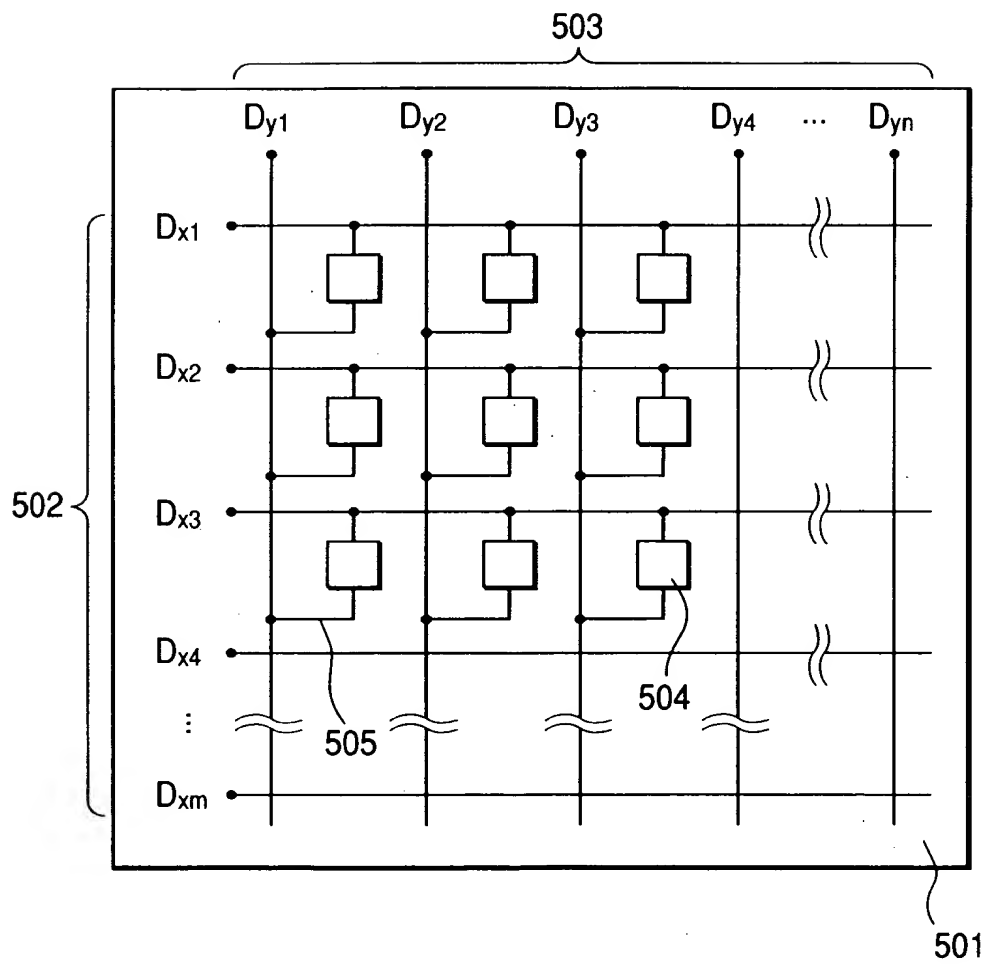


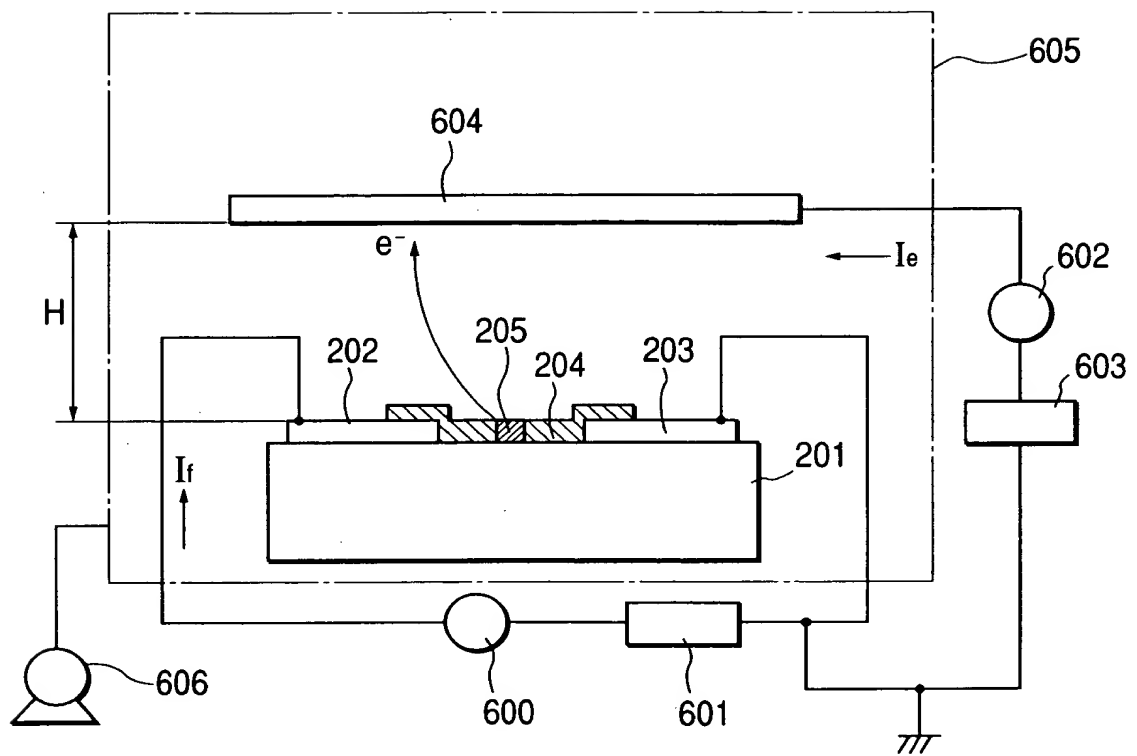
FIG. 6

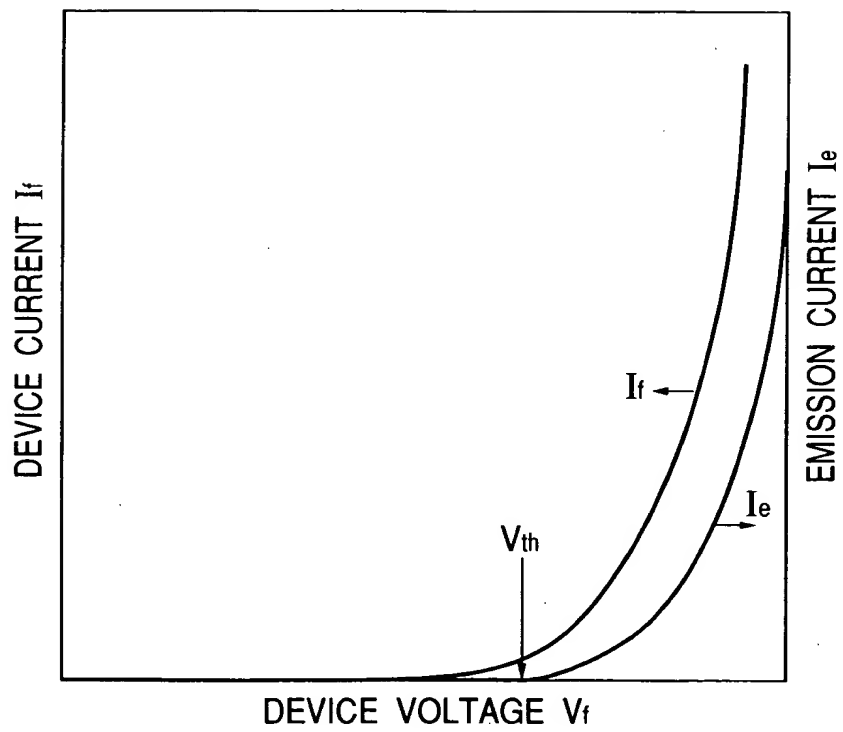
FIG. 7

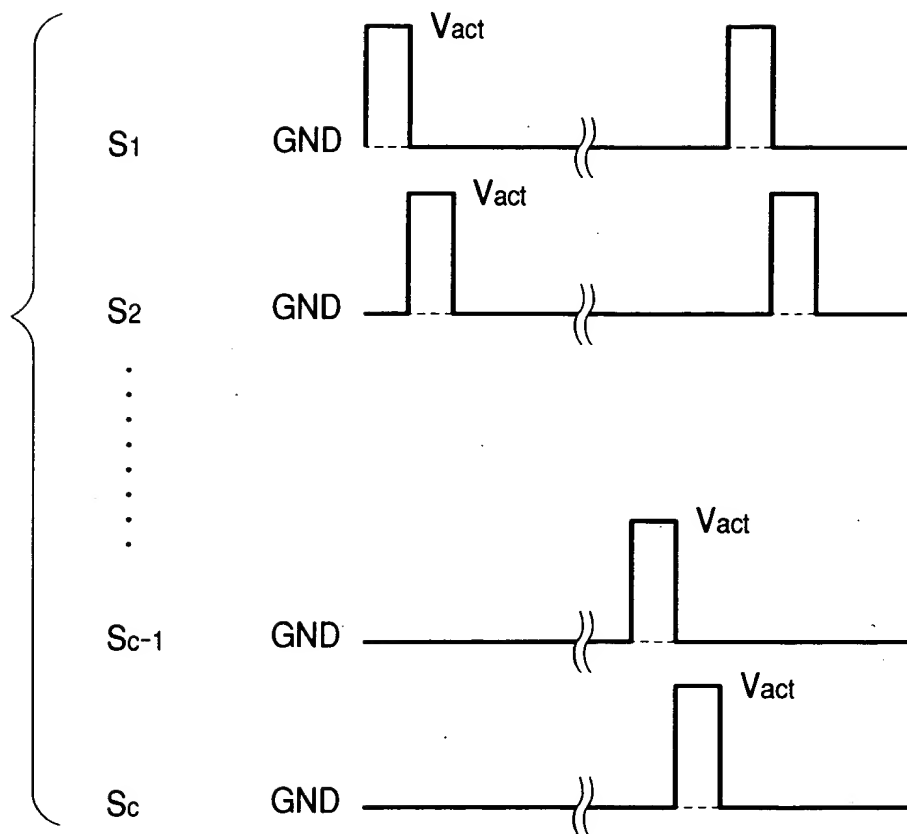
FIG. 8

FIG. 9

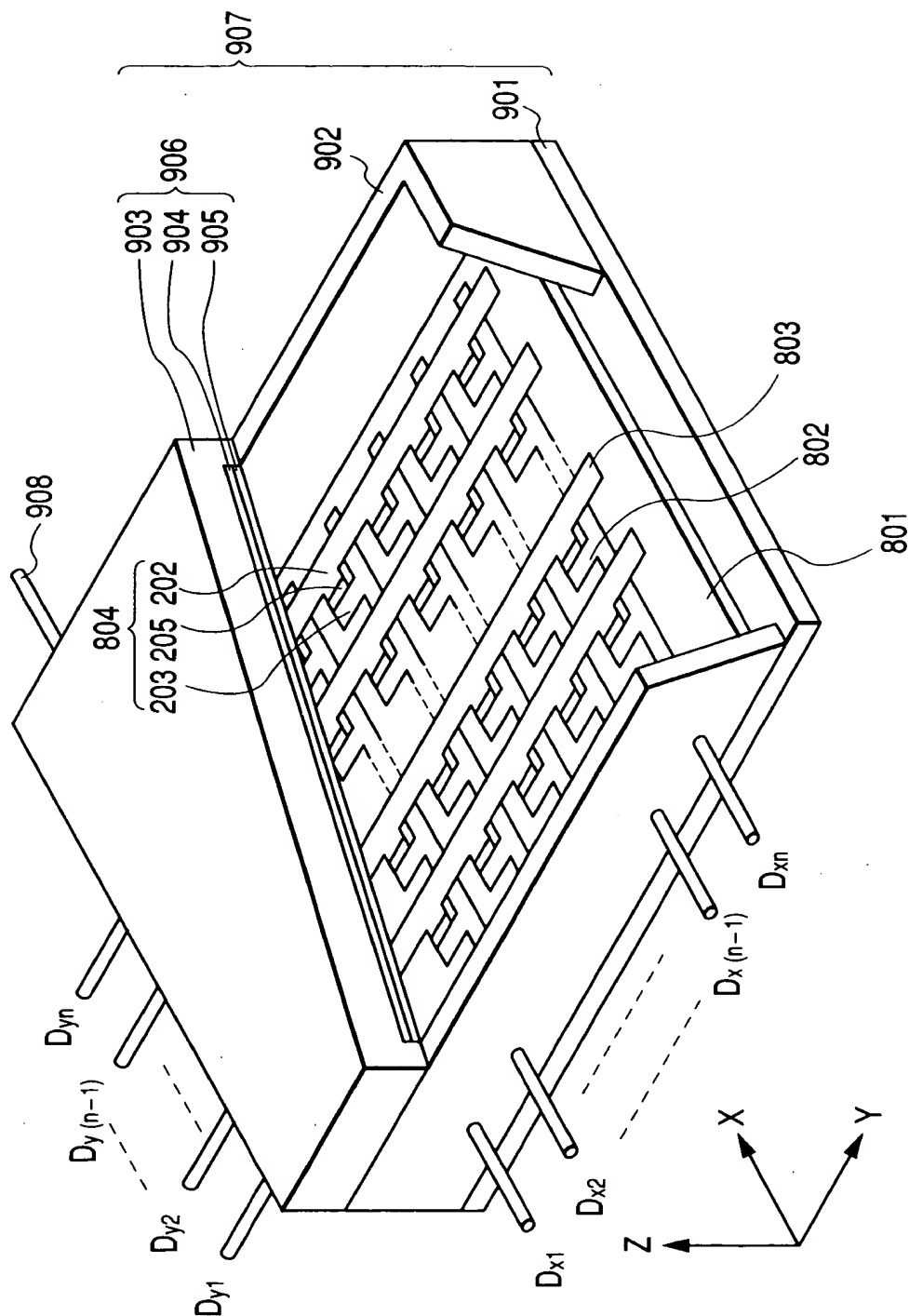


FIG. 10A

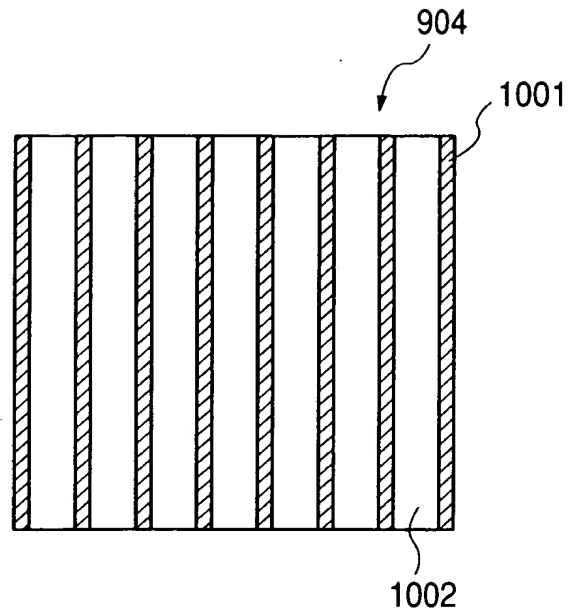


FIG. 10B

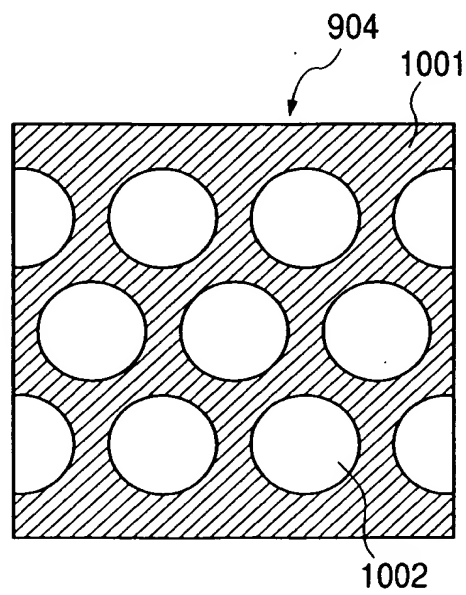


FIG. 11

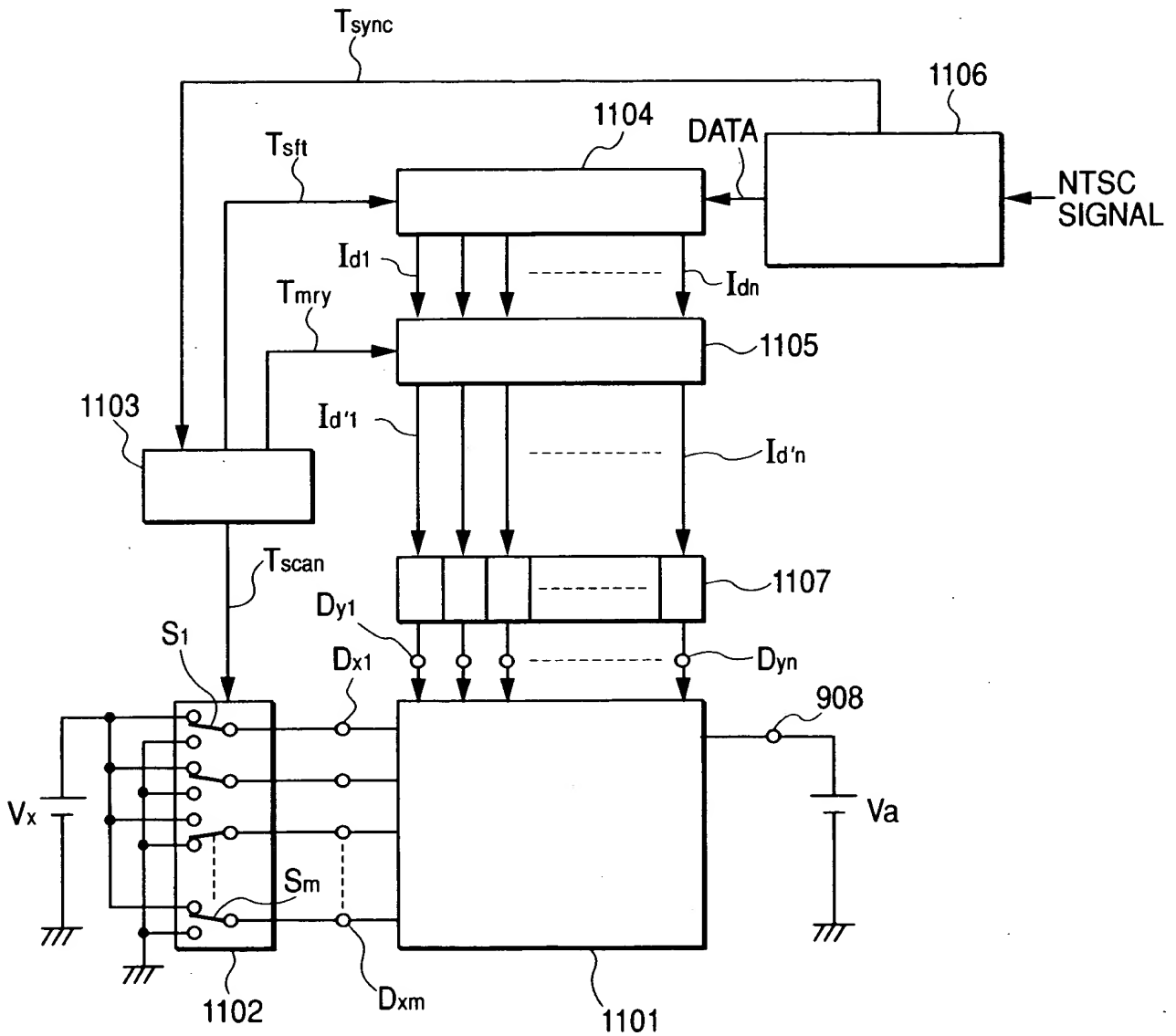


FIG. 12

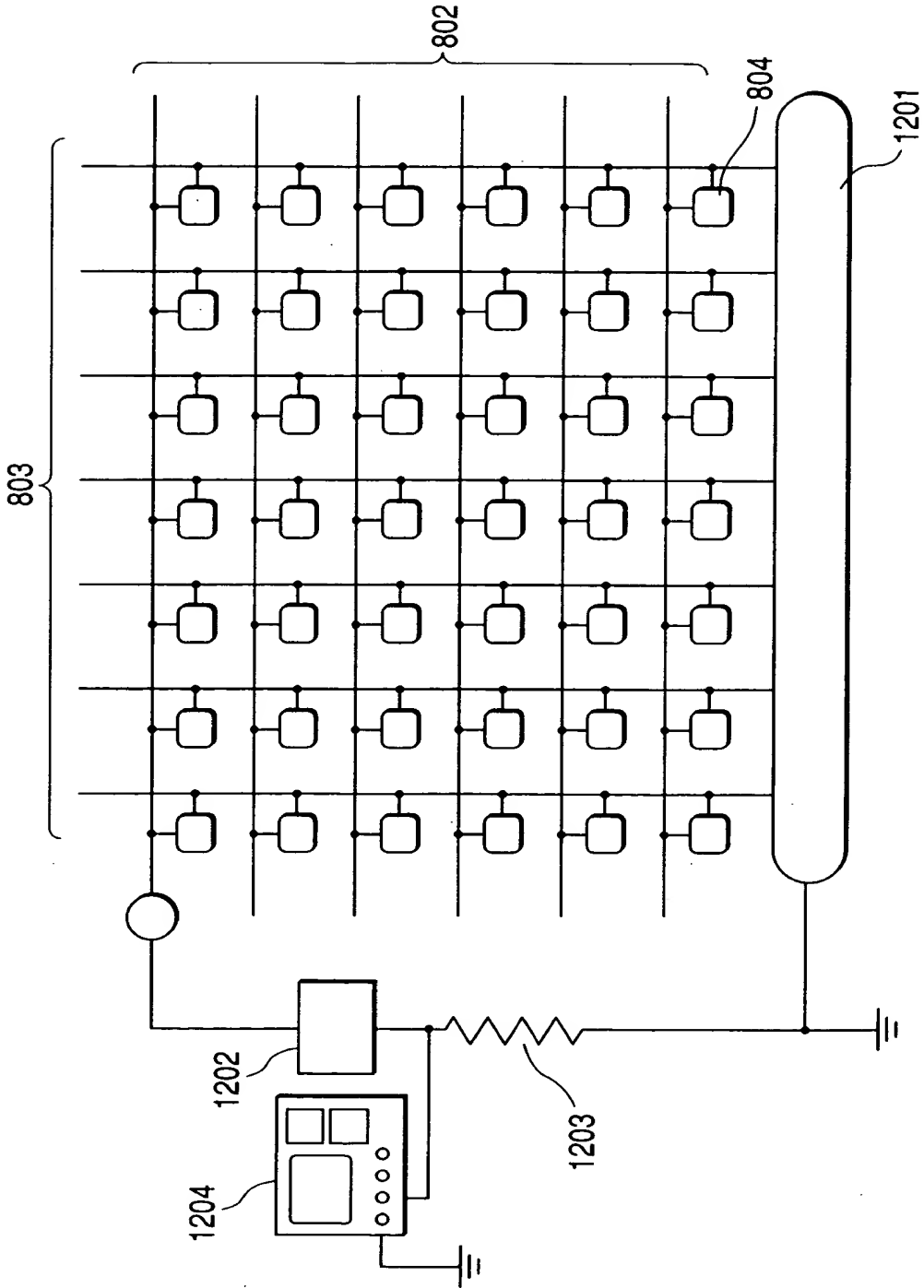


FIG. 13

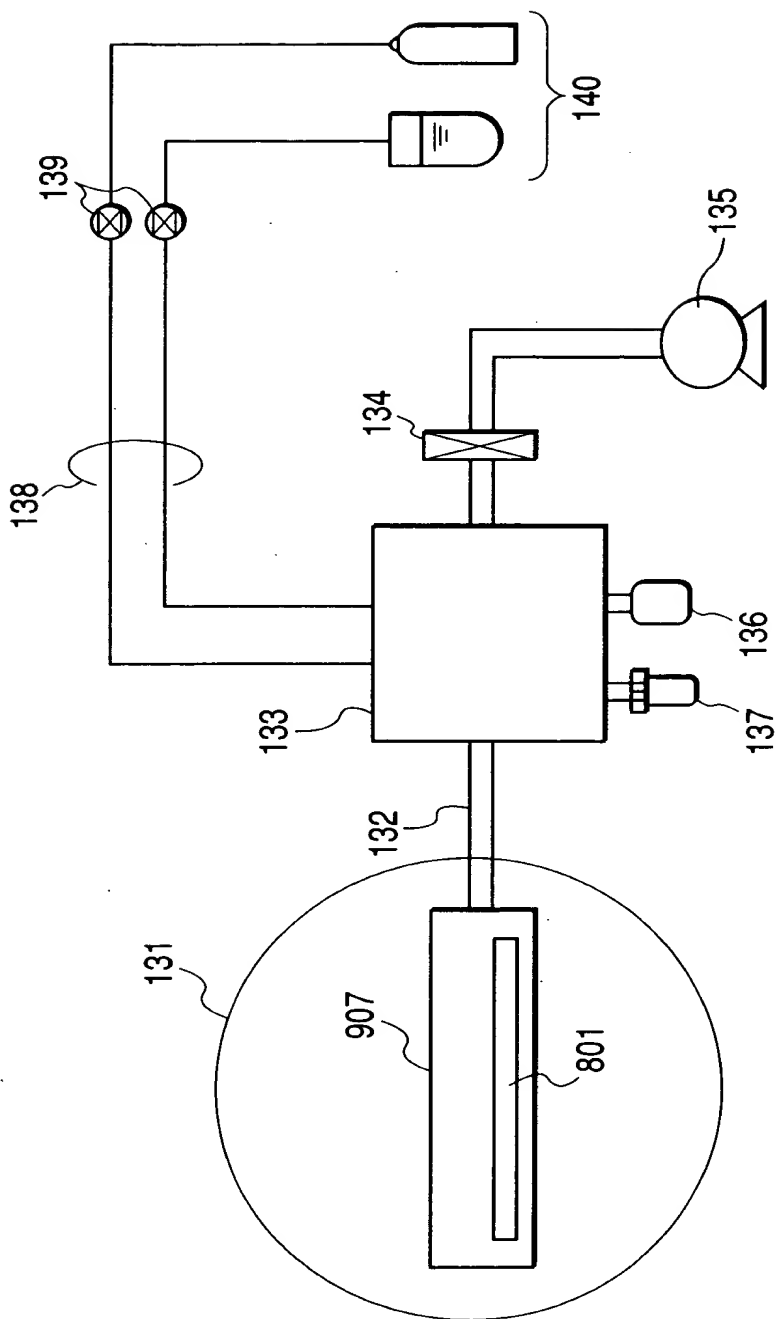


FIG. 14

$$m = a \times b \times c$$

$$S1 : Dy_d, Dy_{d+d}, \dots, Dy_{(a-1)b+d}$$

$$S2 : Dy_{ab+d}, Dy_{b+a+d}, \dots, Dy_{(a-1)b+ab+d}$$

$$\vdots$$

$$S_{c-1} : Dy_{(c-2)ab+d}, Dy_{(c-2)ab+b+d}, \dots, Dy_{(c-2)ab+(a-1)b+d}$$

$$S_c : Dy_{(c-1)ab+d}, Dy_{(c-1)ab+b+d}, \dots, Dy_{(c-1)ab+(a-1)b+d}$$

(d IS NATURAL NUMBER OF 1~b)

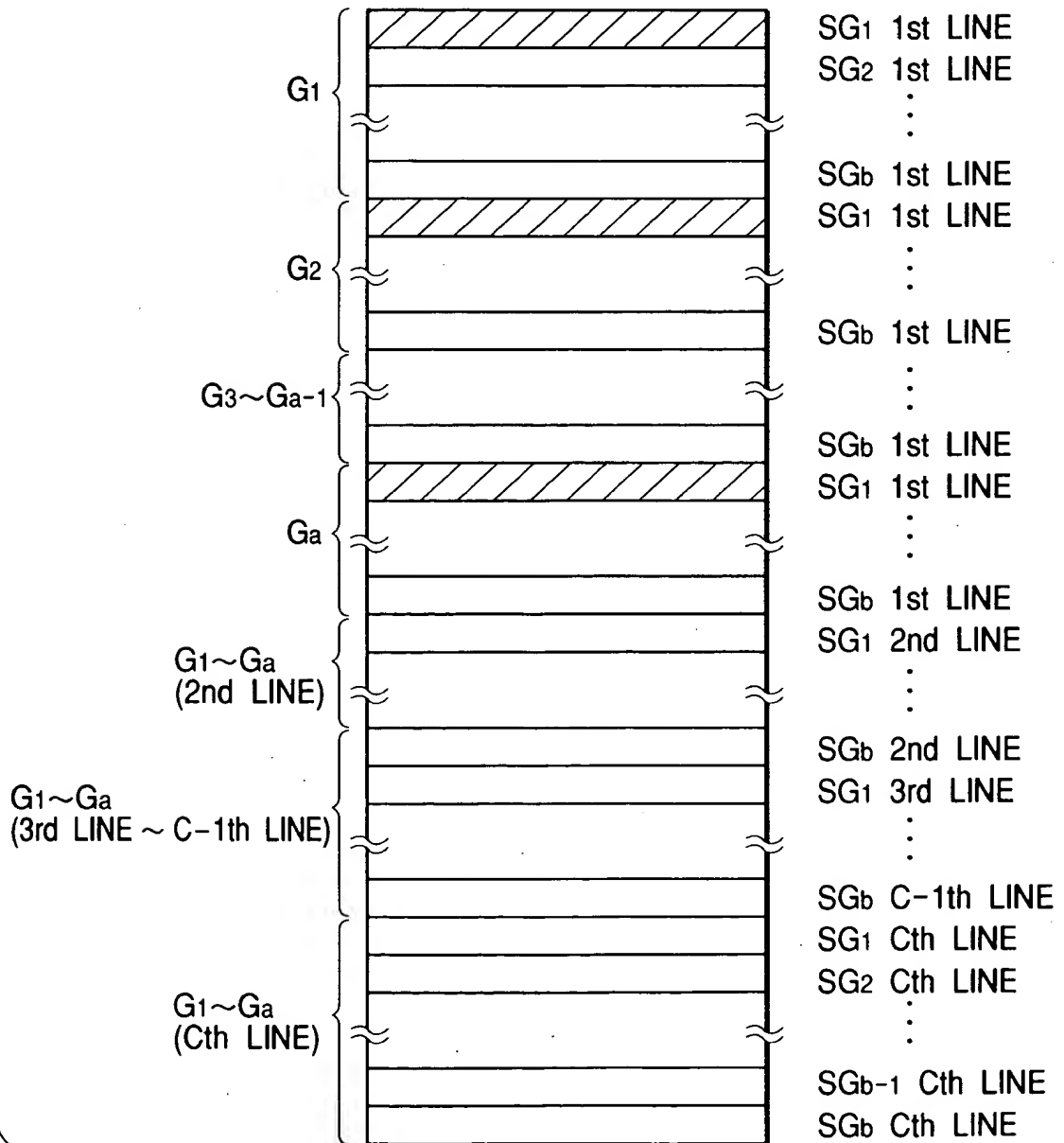


FIG. 15

$$m = e \times a \times b \times c$$

$$S_1 : Dy_d, Dy_{b+d}, \dots, Dy_{(a-1)b+d}$$

$$S_2 : Dy_{ab+d}, Dy_{b+ab+d}, \dots, Dy_{(a-1)b+ab+d}$$

$$\vdots$$

$$S_{c-1} : Dy_{(c-2)ab+d}, Dy_{(c-2)ab+b+d}, \dots, Dy_{(c-2)ab+(a-1)b+d}$$

$$S_c : Dy_{(c-1)ab+d}, Dy_{(-1)ab+b+d}, \dots, Dy_{(c-1)ab+(a-1)b+d}$$

(d IS AN INTEGER OF $1 \sim b$, $abc+1 \sim acb+f$, \dots , $acb(e-1)+1 \sim acb(e-1)+n$)

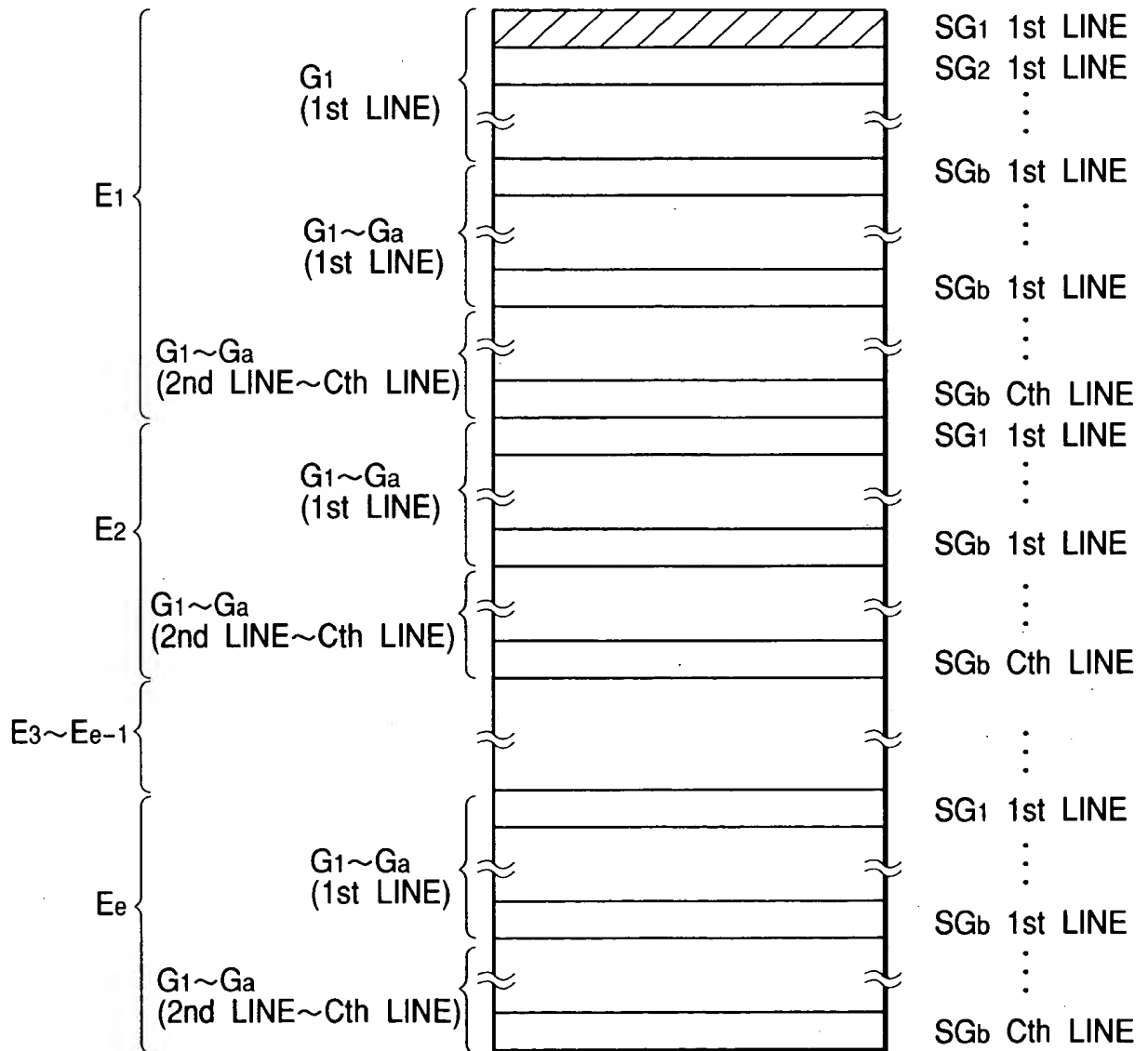


Fig. 19 is a cross-sectional view of a semiconductor device. It shows a substrate 1901 with a trench 1904. A plug 1905 is formed in the trench. The width of the trench is labeled W' and the length of the plug is labeled L .

FIG. 17

